correction 1/24/06

29. (Original) A method for determining the propagation delay of an integrated circuit, comprising:

logically inverting a clock signal, resulting in an inverted clock signal;

delaying the propagation of the inverted clock signal multiple times, resulting in a plurality of delayed inverted clock signals, with each delayed inverted clock signal being delayed a different amount;

forming a plurality of logical AND functions, each logical AND function being associated with one of the plurality of delayed inverted clock signals, each logical AND function generating a logical AND signal representing a logical AND of its associated delayed inverted clock signal and the logical AND signal generated by the logical AND function associated with the immediately preceding delayed inverted clock signal if an immediately preceding delayed inverted clock signal exists; and

storing the logical state of each of the ~~delayed inverted clock~~ logical AND signals at each pulse of the clock signal, resulting in a stored logical state for each of the delayed inverted clock signals.

30 ~~29.~~ (Original) The method of claim 29, wherein the plurality of delayed inverted clock signals is delayed in a linear fashion.

31. (Original) The method of claim 29, further comprising forcing the stored logical state of each of the delayed inverted clock signals to collectively display a single logical transition indicating the propagation delay of the integrated circuit.

32. (Original) The method of claim 29, further comprising tuning the speed of a critical signal based on the stored logical state for each of the delayed inverted clock signals.